

IN THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the above-referenced application:

1. (Canceled)
2. (Currently amended) The method of claim ~~1~~ 5, further comprising the steps of:
 - polishing the upper surface of the epitaxial layer so that the upper surface of the epitaxial layer is substantially planar; and
 - forming an insulating layer on at least a portion of the upper surface of the semiconductor wafer.
3. (Currently amended) The method of claim ~~1~~ 5, wherein the step of forming the at least one trench comprises:
 - forming an insulating layer on at least a portion of the epitaxial layer;
 - forming at least one opening in the insulating layer corresponding to the at least one trench; and
 - etching through the epitaxial layer to at least partially expose the substrate.
4. (Currently amended) The method of claim ~~1~~ 5, wherein the at least one trench comprises a v-groove.
5. (Currently amended) ~~The method of claim 1,~~ A method of forming a semiconductor structure in a semiconductor wafer, the method comprising the steps of:
 - forming an epitaxial layer on at least a portion of a semiconductor substrate of a first conductivity type;
 - forming at least one trench through the epitaxial layer to at least partially expose the substrate;

doping at least one or more sidewalls of the at least one trench with an impurity of a known concentration level so as to form a low-resistance electrical path between an upper surface of the epitaxial layer and the substrate; and

substantially filling the at least one trench with a filler material;

wherein the step of doping at least one or more sidewalls of the at least one trench with an impurity comprises:

cleaning the sidewalls of the at least one trench to substantially remove any organic material in the at least one trench;

predepositing the impurity on at least one or more sidewalls of the at least one trench;

and

driving in the impurity.

6. (Original) The method of claim 5, wherein the impurity comprises boron.

7. (Original) The method of claim 5, wherein the step of driving in the impurity comprises heating the semiconductor wafer for a predetermined period of time.

8. (Original) The method of claim 7, wherein the step of heating the semiconductor wafer comprises heating the semiconductor wafer at a temperature in a range of about 900 degrees Celsius to about 1200 degrees Celsius for a duration of about one hour.

9. (Original) The method of claim 5, wherein the step of predepositing the impurity on at least one or more sidewalls of the at least one trench comprises growing an impurity-rich oxide on at least one or more sidewalls of the at least one trench.

10. (Currently amended) The method of claim 5, wherein the step of substantially filling the at least one trench comprises depositing a semiconductor material in the at least one trench so as to substantially fill the trench.

11. (Currently amended) The method of claim + 5, wherein the filler material comprises polysilicon material.

12. (Currently amended) The method of claim + 5, further comprising the step of forming at least one insulating layer on at least a portion of the epitaxial layer.

13. (Currently amended) The method of claim + 5, further comprising the step of:
forming an active device in the epitaxial layer proximate the upper surface of the epitaxial layer, the active device being in electrical connection with a first end of the at least one trench, a second end of the at least trench being electrically connected to the substrate.

14. (Original) The method of claim 13, wherein the active device comprises a metal-oxide-semiconductor device.

15. (Currently amended) The method of claim + 5, further comprising the steps of:
forming an insulating layer on at least a portion of the upper surface of the epitaxial layer;
forming a gate on at least a portion of the insulating layer;
forming first and second source/drain regions of a second conductivity type in the epitaxial layer proximate the upper surface of the epitaxial layer, the first source/drain region being spaced laterally from the second source/drain region, the gate being formed at least partially between the first and second source/drain regions, the first source/drain region being electrically connected to a first end of the at least one trench and a second end of the at least one trench being electrically connected to the substrate.

16. (Currently amended) The method of claim + 5, wherein the step of forming at least one trench comprises forming at least two trenches through the epitaxial layer to at least partially expose the substrate, the at least two trenches being spaced about five microns apart relative to one another.

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17. (Currently amended) The method of claim \pm 5, wherein the at least one trench is formed about one to two microns in width.

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Canceled)